

#34
OKN
13/24/91
Our Ref.: 042390.P4537

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of:

Melik Isbara

Serial No.: 08/925,868

Filed: September 9, 1997

For: **METHOD AND APPARATUS
FOR INTERFACING MIXED VOLTAGE
SIGNALS**

Examiner: Kenneth B. Wells

Art Group: 2816

RECEIVED
BOARD OF PATENT APPEALS AND INTERFERENCES
OCT 22 2001
TECHNICAL DIVISION
CIVIL 714

REPLY BRIEF

Box: Board of Patent Appeals and Interferences
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the Examiner's answer mailed August 16, 2001 in connection with the above-identified application, Appellant submits the following reply.

Under the section entitled "Grounds of Rejection" in the Examiner's answer, it is contended that the replacement of a discrete resistor with a continuously-on biased FET is notoriously well known in the art. In addition, it is stated that there is an obvious motivation to make such a replacement to save chip real estate, since

discrete resistors take up more space than integrated FETs. Appellant respectfully disagrees with these contentions for the following reasons.

Firstly, although a continuously-on biased FET may provide a relatively predictable resistance, this does not teach or suggest the Examiner's contention that in applications in which a discrete resistor is used, a continuously-on biased FET would work just as well. In support of this contention, the Examiner's answer, on page 5, cites several references which allegedly show the equivalence of a discrete resistor and a continuously biased FET. Appellant now addresses each of these in turn.

U. S. Patent No. 5,130,571 to Carroll ("Carroll") seeks to optimize speed and charge injection parameters of a switched capacitor circuit. A typical switch capacitor circuit 10 is shown in Fig. 1 of Carroll, where the circuit includes a n-channel transistor M1 connected between an input V_{in} and the output V_{out} . Carroll then states:

Since transistor M1 may be thought of as an equivalent resistor $R_{eq} = R(M1)$ for $V_{in} < V_{control} - V_{tn}$, the switched capacitor circuit 10 shown in Fig. 1 may be illustrated as an RC circuit 10' during a sample time t_s , as shown in Fig. 2.

Carroll, column 1 lines 20-24. Contrary to the Examiner's contention, this does not teach or suggest that a discrete resistor can be readily replaced with a continuously-on biased FET. Rather, the emphasized portion of Carroll only suggests that in a switched capacitor circuit where a transistor is used in a switching sense, the behavior of the transistor during one portion of the switching cycle (as

shown in Fig. 3 of Carroll) can be represented as an equivalent resistance. It is improper to generalize from this narrow teaching that one of ordinary skill in the art would be readily motivated to replace a resistor in a circuit design with a continuously biased FET.

U. S. Patent No. 4,970,478 to Townley ("Townley") is directed to a matched microwave variable attenuator. This variable attenuator is a sequence of LRC components in which a shunt resistance is obtained by using a biased FET, because the biased FETs exhibit resistive changes with properly applied DC voltage and are thus useful as variable resistors. Townley, column 1 lines 15-20. This variable resistance is particularly useful in microwave applications, because of the desire to provide an attenuator whose impedance matches that of the transmission line. Townley, column 1 lines 21-24. It is important to note here that, now referring to Fig. 6 of Townley, the transistor 26 is used to present a variable shunt resistance which, in all circumstances, attenuates an input microwave signal across its source drain terminals. This configuration of the variable resistance coupled in parallel with a capacitor is similar to the combination $R_2 - C_2$ in Nelson, and not the combination of $R_1 - C_1$. Thus, although Townley might arguably suggest that, for microwave applications, a parallel combination of $R_2 - C_2$ as in Nelson be modified to form the combination shown in Fig. 6 of Townley, that would not teach or suggest that the same modification would work or even be desirable for the series connection of the combination $R_1 - C_1$ in Nelson. This distinction is important, because Appellant's claims are directed to the configuration of a transistor such that

the input terminal is coupled to receive the binary signals and the output terminal is coupled to deliver the binary signals, i.e. a series type of connection. This series vs. shunt distinction is also apparent when it is recognized that in Townley, both the input and output signals of the attenuator are measured with respect to the same electrical node which is shorted to the lower terminal of the transistor 26 (see Fig. 6 of Townley) - a shunt-type connection. Accordingly, Townley does not teach or suggest that a discrete resistor in a series configuration be replaced by a biased FET.

U. S. Patent No. 5,604,364 to Ohmi et al. ("Ohmi") is directed to a photoelectric converter. Ohmi discusses an analysis of circuit operation by modeling a transistor 40-40" as an equivalent resistance R_m . Ohmi, Fig. 9 and column 4 lines 66-67 and column 21 lines 62 to column 22 line 1. Again, this does not suggest the contention made in the Examiner's answer of replacing an actual discrete resistor with a transistor in an attenuator circuit.

The above discussion of Carroll, Townley, and Ohmi makes it clear that replacing a discrete resistor with a continuously-on biased FET is not notoriously well known in the art for all circuit applications. Although it is true, such as described in Townley, that in some cases, namely a number of shunt resistances in a LRC microwave attenuator, the discrete resistor could be replaced by a variable resistance transistor to make it easier to match the impedance of the attenuator with that of a transmission line, this does not provide the general teaching that in all instances, a discrete, series connected resistor may be readily replaced by a continuously biased FET. It would be an improper use of hindsight to argue, as has

been done in the Examiner's answer, that it is well known in the art to replace such a connected discrete resistor with a continuously-on biased FET.

A second point of issue with the Examiner's answer is that even if one of ordinary skill in the art would know that each instance of a discrete resistor could be replaced by a continuously biased FET, there is no obvious motivation to make such a replacement to modify the attenuator of Nelson.

According to the Examiner's answer on page 4, motivation to make such a replacement would be to save chip real estate, since discrete resistors take up more space than integrated FETs acting as resistance elements. According to the Examiner's answer, on page 4, use of a series resistor between a gate bias voltage and the gate of the FET, for the purpose of controlling the on level of the FET and thereby controlling the resistance value of the FET, is also known in the art. However, this argument fails because the motivation to save chip real estate is not met by replacing a single resistor with a combination of a FET and gate bias resistor. If an additional resistance is also needed to make the transistor operate as an equivalent resistance, then where is the savings in chip real estate? Furthermore, there is the additional requirement of providing access to a suitable voltage source to bias the gate of the transistor. Thus, it is not at all clear that one of ordinary skill in the art would be motivated to replace a single, discrete resistor as in Nelson with a FET, a gate resistor, and additional metal traces to access a suitable voltage source, in the hope of making more efficient use of chip real estate.

In view of the foregoing, Appellant respectfully requests that the Board
overturn the obviousness rejection of the claims.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

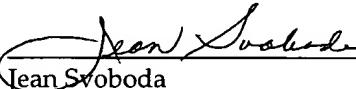


Farzad E. Amini, Reg. No. 42,261

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited
with the United States Postal Service as first class mail in an
envelope addressed to: Assistant Commissioner for Patents,
Washington, D.C. 20231 on October 16, 2001.


Jean Svoboda

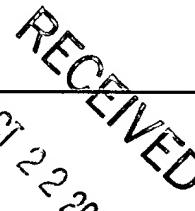
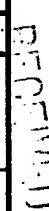
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FORM

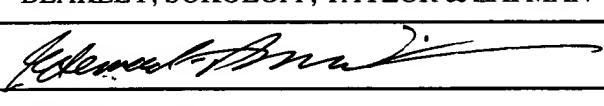
(to be used for all correspondence after initial filing)

| | | | |
|--|----|-----------------------------|-------------------|
| | | Application Number | 08/925,868 |
| | | Filing Date | September 9, 1997 |
| | | First Named Inventor | Melik Isbara |
| | | Group Art Unit | 2816 |
| | | Examiner Name | Kenneth B. Wells |
| Total Number of Pages in This Submission | 10 | Attorney Docket Number | 42390P4537 |

ENCLOSURES (check all that apply)

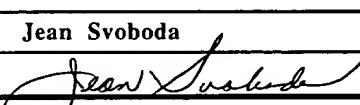
| | | |
|--|---|---|
| <input checked="" type="checkbox"/> Fee Transmittal Form | <input type="checkbox"/> Assignment Papers <i>(for an Application)</i> | <input type="checkbox"/> After Allowance Communication to Group |
| <input type="checkbox"/> Fee Attached | <input type="checkbox"/> Drawing(s) | <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences |
| <input type="checkbox"/> Amendment / Response | <input type="checkbox"/> Licensing-related Papers | <input checked="" type="checkbox"/> Appeal Communication to Group <i>(Appeal Notice, Brief, Reply Brief)</i> |
| <input type="checkbox"/> After Final | <input type="checkbox"/> Petition | <input type="checkbox"/> Proprietary Information |
| <input type="checkbox"/> Affidavits/declaration(s) | <input type="checkbox"/> Petition to Convert a Provisional Application | <input type="checkbox"/> Status Letter |
| <input type="checkbox"/> Extension of Time Request | <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address | <input checked="" type="checkbox"/> Other Enclosure(s) <i>(please identify below):</i> |
| <input type="checkbox"/> Express Abandonment Request | <input type="checkbox"/> Terminal Disclaimer | |
| <input type="checkbox"/> Information Disclosure Statement | <input type="checkbox"/> Request for Refund | |
| <input type="checkbox"/> Certified Copy of Priority Document(s) | <input type="checkbox"/> CD, Number of CD(s) _____ | |
| <input type="checkbox"/> Response to Missing Parts/ Incomplete Application | | |
| <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53 | | |
| <p style="text-align: center;">Remarks</p> <p style="text-align: center;">REPLY BRIEF</p> | | |
| Return receipt postcard  OCT 22 2001 BOARD OF PATENT APPEALS AND INTERFERENCES TECHNICAL CENTER 2025  | | |

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

| | |
|-------------------------|--|
| Firm or Individual name | Farzad E. Amini, Reg. No. 42,261 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN |
| Signature |  |
| Date | October 16, 2001 |

CERTIFICATE OF MAILING (OR TRANSMISSION)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on this date: **October 16, 2001**

| | |
|-----------------------|---|
| Typed or printed name | Jean Svoboda |
| Signature |  |
| Date | 10/16/01 |

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL

for FY 2002

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT (\$)

Complete if Known

| | |
|------------------------|------------------|
| Application Number | 08/925,868 |
| Filing Date | 09/09/97 |
| First Named Inventor | Melik Isbara |
| Examiner Name | Kenneth B. Wells |
| Group Art Unit | 2816 |
| Attorney Docket Number | 42390P4537 |

METHOD OF PAYMENT (check one)

1. The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number

Deposit Account Name

Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

Applicant claims small entity status. See 37 CFR 1.27

2. Payment Enclosed:

Check Money Order Other

FEE CALCULATION

1. FILING FEE

| Large Entity | Small Entity | Fee Description | Fee Paid |
|---------------|---------------|-----------------|---------------------------|
| Fee Code (\$) | Fee Code (\$) | Fee Description | Fee Paid |
| 101 | 740 | 201 | 370 Utility filing fee |
| 106 | 330 | 206 | 165 Design filing fee |
| 107 | 510 | 207 | 255 Plant filing fee |
| 108 | 740 | 208 | 370 Reissue filing fee |
| 114 | 160 | 214 | 80 Provisional filing fee |

SUBTOTAL (1) (\$)

2. CLAIMS

| Total Claims | Independent Claims | Extra | Fee from below | Fee Paid |
|----------------------|----------------------|----------------------|----------------------|----------------------|
| <input type="text"/> |
| = | = | X | = | = |

Multiple Dependent Claims

| Large Entity | Small Entity | Fee Description |
|---------------|---------------|---|
| Fee Code (\$) | Fee Code (\$) | Fee Description |
| 103 | 18 | 203 9 Claims in excess of 20 |
| 102 | 84 | 202 42 Independent claims in excess of 3 |
| 104 | 280 | 204 140 Multiple Dependent claim |
| 109 | 84 | 209 42 Reissue independent claims over original patent |
| 110 | 18 | 210 9 Reissue claims in excess of 20 and over original patent |

SUBTOTAL (2) (\$)

* or number previously paid, if greater. For Reissues, see above

3. ADDITIONAL FEE

| Large Entity | Small Entity | Fee Description | Fee Paid |
|---------------|---------------|---|----------|
| Fee Code (\$) | Fee Code (\$) | Fee Description | Fee Paid |
| 105 | 130 | 205 65 Surcharge - late filing fee or oath | |
| 127 | 50 | 227 25 Surcharge - late provisional filing fee or cover sheet | |
| 139 | 130 | 139 130 Non-English specification | |
| 147 | 2,520 | 147 2,520 For filing a request for ex parte reexamination | |
| 112 | 920 | 112 920 Requesting publication of SIR prior to Examiner action | |
| 113 | 1,840 | 113 1,840 Requesting publication of SIR after Examiner action | |
| 115 | 110 | 215 55 Extension for response within first month | |
| 116 | 400 | 216 200 Extension for response within second month | |
| 117 | 920 | 217 460 Extension for response within third month | |
| 118 | 1,440 | 218 720 Extension for response within fourth month | |
| 128 | 1,960 | 228 980 Extension for response within fifth month | |
| 119 | 320 | 219 160 Notice of Appeal | |
| 120 | 320 | 220 160 Filing a brief in support of an appeal | |
| 121 | 280 | 221 140 Request for oral hearing | |
| 138 | 1,510 | 138 1,510 Petition to institute a public use proceeding | |
| 140 | 110 | 240 55 Petition to revive - unavoidably | |
| 141 | 1,280 | 241 640 Petition to revive - unintentionally | |
| 142 | 1,280 | 242 640 Utility issue fee (or reissue) | |
| 143 | 460 | 243 230 Design issue fee | |
| 144 | 620 | 244 310 Plant issue fee | |
| 122 | 130 | 122 130 Petitions to the Commissioner | |
| 123 | 50 | 123 50 Petitions related to provisional applications | |
| 126 | 180 | 126 180 Submission of Information Disclosure Stmt | |
| 581 | 40 | 581 40 Recording each patent assignment per property (times number of properties) | |
| 146 | 740 | 246 370 Filing a submission after final rejection (37 CFR 1.129(a)) | |
| 149 | 740 | 249 370 For each additional invention to be examined (37 CFR 1.129(b)) | |
| 179 | 740 | 279 370 Request for Continued Examination (RCE) | |
| 169 | 900 | 169 900 Request for expedited examination of a design application | |

Other fee (specify) _____

SUBTOTAL (3) (\$)

* Reduced by Basic Filing Fee Paid

| | | | | |
|-----------------------|---|---------|--------------------------|-----------------|
| SUBMITTED BY | | | Complete (if applicable) | |
| Typed or Printed Name | Farzad E. Amini, Reg. No. 42,261 | | | Reg. Number |
| Signature |  | | | Date 10/16/2001 |
| | Deposit Account User ID | 02-2666 | | |

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.